REMARKS

The Office Action dated May 31, 2005 has been received and carefully considered. In this response, claims 1, 8, 11, 13, 38, 41, 43, 45, 46 and 48 have been amended and claims 6, 7, 21-27, 39, 40, 44, 47, 49 and 50 have been canceled without prejudice. Support for the amendments to the claims may be found in the specification and figures as originally filed. Entry thereof and reconsideration of the outstanding rejections therefore is respectfully requested.

Allowance of Claims 28-31, 32, 34-37 and 51-53

The Applicants note with appreciation the indication at page 10 of the Office Action that claims 28, 31, 32, 34-37 and 51-53 are allowed.

Indefinite Rejection of Claims 8-13, 47 and 50

At page 2 of the Office Action, claims 8-13, 47 and 50 were rejected under 35 U.S.C. Section 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter regarded as the invention. Specifically, the Office Action asserted that there is insufficient antecedent basis for the feature "the number of bits used to represent multimedia data" in the identified dependent claims. The Applicants have amended the claims consistent with the Office Action's remarks by clarifying that it is "the number of bits used to represent a multimedia data processed by the system." Withdrawal of this rejection therefore is respectfully requested.

Failure to Provide a Rejection for Claims 22-27 and 48

The Office Action does not state any grounds for rejecting claims 22-27 and 48 nor does the Office Action cite any references or provide any rationale for rejecting claims 22-48. In fact, other than the general listing at page 1 of the Office Action, the Office Action is silent with respect to claims 22-27 and 48. Claims 22-27 have been canceled and claim 48 has been rewritten in independent form including all of the features of the base claim 1 and intervening claim 7 as previously presented. No additional features have been added nor have any features

been removed. Thus, the scope of claim 48 remains unchanged even though claim 48 has been placed in independent form. As the Office Action does not provide a *prima facie* case for rejecting claim 48, the Applicants respectfully request that the Office issue another office action with an indication of the allowance of claim 48 or with an appropriate rejection of claim 48 that provides both the grounds for rejection and the rationale for rejection.

Rejections of Claims 1, 8-10, 16-18, 45 and 46

At page 3 of the Office Action, claims 1 and 45 were rejected under 35 U.S.C. Section 102(b) as being anticipated by Paver (U.S. Patent No. 6,049,882). At page 5 of the Office Action, claims 8-10 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over Paver in view of Bucher (U.S. Patent No. 6,678,737). At page 6 of the Office Action, claims 16-18 and 46 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over Paver in view of Bucher and further in view of Gupta (U.S. Patent No. 5,996,083). These rejections are respectfully traversed.

Claim 1, from which claims 8-10, 16-18, 45 and 46 depend, has been amended to remove reference to the features of the operating characteristic comprising a buffer fullness or a type of instructions. Accordingly, claim 1 presently recites the features of identifying a rate of change in a number of pending instructions stored in an instruction buffer, and adjusting a system characteristic based on the rate of change in the number of pending instructions, wherein a power consumption of a system is modified based on the system characteristic. With respect to claim 1, the Office Action asserts that Paver discloses an apparatus and method comprising:

> a. identifying [by counting number of instructions waiting in queue] an operating characteristic [delay (cycle time)] of an instruction buffer [instruction buffer/FIFO/register, FIG. 3], the operating characteristics comprising at least one of a buffer fullness [register stalled represents fullness as it can not except data until register is empty] [col. 2, lines 40-56, col. 4, lines 48-52], a rate of change of a number of pending instructions stored [by counting number of instructions waiting in a queue per cycle time] in the instruction buffer [col. 5, lines 43-56, col. 6, lines 54-57, 63-65], and
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> b. adjusting a system characteristic [system performance] based on the operating characteristic [delay (cycle time)], wherein power consumption is modified [adjusted] based on the system characteristic [system performance] [col. 5, lines 6-67, col. 6, lines 1-14, FIGs. 3, 8].

Office Action, pp. 3-4.

With specific reference to identifying a rate of change in a number of pending instructions, the Office Action asserts that the passage of Paver at col. 5, line 60-col. 6, line 14 discloses identifying a rate of change in the number of pending instructions "by counting the number of instructions waiting in a queue per cycle time." *Office Action*, p. 9. For ease of reference, this relied-upon passage of Paver is reproduced below in its entirety:

> As shown in FIG. 8, a variable cycle time that is used to control power consumption is based on an instruction queue length. A power control device 802 dynamically adjusts the system performance (e.g., cycle time) and power consumption depending on workload requirements. In the first preferred embodiment, the system performance adjustment is achieved by changing a variable delay in one processing stage e.g., instruction fetch).
>
> As shown in FIG. 8, an instruction queue length is used to indicate the processor workload requirements. A counter is used to count the number of elements (e.g., instructions) waiting in a queue to be processed. The variable cycle time is then controlled by the power control device 802 as a function of queue length. As the "queue length" gets longer and there is more work to do, the delay (e.g., cycle time) is reduced. Accordingly, the system power consumption and system performance is increased. As the "queue length" of work becomes smaller, the cycle time is increased to decrease the power consumption and the system performance. Thus, power consumption corresponds to the amount of work (e.g., execution requirements of the processor) to be done.

Paver, col. 5, line 60 – col. 6, line 14.

However, the Applicants submit that Paver does not support this assertion as the cited passage of Paver merely discloses that a variable cycle time of the system of Paver is controlled "as a function of queue length," where "a counter is used to count the number of elements (e.g., instructions) waiting in the queue to be processed," and "as the 'queue length' gets longer and as there is more work to do, the delay (e.g., cycle time) is reduced . . . [a]s the 'queue length' of work becomes smaller, cycle time is increased . . ." *Id.*. Although this passage discloses counting the number of elements/instructions waiting to be processed, neither this passage nor any other passage of Paver discloses that a change in the number of elements/instructions waiting to be processed (and, consequently, the rate of such a change) is considered in any manner. Thus, Paver fails to disclose identifying a rate of change in the number of pending instructions stored in the in any manner. Paver therefore necessarily fails to disclose adjusting a system

characteristic of a system based on the rate of change in the number of pending instructions as recited by claim 1. The Office Action does not assert that Bucher or Gupta disclose or suggest any of these features. Accordingly, the Applicants respectfully submit that the Office Action fails to establish that the cited references, alone or in combination, disclose or suggest each and every feature of claim 1, as well as each and every feature of claims 8-10, 16-18, 45 and 46 at least by virtue of their dependency from claim 1. Moreover these dependent claims recite additional features neither disclosed nor suggested by the cited references.

In view of the foregoing, it is respectfully submitted that the rejections of claims 1, 8-10, 16-18, 45 and 46 are improper and the withdrawal of these rejections therefore is respectfully requested.

Rejections of Claims 11-13

At page 3 of the Office Action, claim 11 was rejected under 35 U.S.C. Section 102(b) as being anticipated by Paver. At page 5 of the Office Action, claim 13 was rejected under 35 U.S.C. Section 103(a) as being unpatentable over Paver in view of Bucher. At page 6 of the Office Action, claim 12 was rejected under 35 U.S.C. Section 103(a) as being unpatentable over Paver in view of Bucher and further in view of Gupta. These rejections are respectfully traversed.

Claim 11, from which claims 12 and 13 depend, has been rewritten so as to include all of the features of base claim 1 as previous presented. No additional features have been added nor have any features been removed. Thus, the scope of claim 11 remains unchanged even though claim 11 has been placed in independent form.

Claim 11 recites the features of adjusting a system characteristic based on an operating characteristic, wherein a power consumption of a system is modified based on the system characteristic and *wherein adjusting the system characteristic includes modifying a clock speed.* With respect to claim 11, the Office Action asserts that "Paver teaches adjusting the system characteristic including modifying s [sic] clock speed (frequency)(col. 5, lines 41-56)." *Office Action*, p. 4; *see also Office Action*, p. 7 (discussing the "cycle time" of Paver). For ease of reference, the cited passage of Paver at col. 5, lines 41-56 is reproduced in its entirety below:

$E = \frac{1}{2} CV^2 \times$ frequency

In the above equation, E=energy, C=capacitance, V=voltage and frequency=1/cycle time.

In self-timed systems, when the cycle time is increased, the frequency and the power consumption are reduced. Therefore, according to preferred embodiments of the present invention, power consumption of a self-time system can be controlled by adjusting the cycle time of a critical functional unit or element of the system.

Using the above-described example of instruction fetch, the processor executes priority work at a first speed or full speed. However, when the processor is idling (e.g., busy waiting), then the processor executes at a second speed or reduced speed. Accordingly, the system performance is reduced at the second speed by increasing the cycle time of the instruction fetch stage. Consequently, the self-timed system power consumption is reduced at the second speed.

Paver, col. 5, lines 40-56.

From the comments in the Office Action and its reliance on the above-reproduced passage of Paver, it appears that the Office Action considers an adjustment of the "cycle time" of Paver as equivalent to the feature of modifying a clock speed as recited by claim 11. The Applicants respectfully submit that the Office Action has misinterpreted the meaning of the term "cycle time" as utilized by Paver.

The techniques of Paver are directed to an asynchronous system (also referred to by Paver as a "self-timed system"). *See Paver*, Title; *see also Id.*, col. 1., lines 49-50, col. 4, lines 28-44, col. 5, lines 11-12, col. 6, lines 59-60; *see also Id.*, claims 1-25. As described by Paver, asynchronous systems "use functional units having an asynchronous interface protocol to pass data and control information." *Paver*, col. 1, lines 61-64. Paver contrasts its asynchronous systems with synchronous systems that "apply a fixed time step signal (i.e., a clock signal) to the functional units to ensure synchronized execution." *Paver*, col. 1, lines 24-26. Paver characterizes "the use of a fixed time clock signal (i.e., a clock signal) in synchronous systems" as "restrict[ing] the design of the functional unit," whereas "self-timed systems, also known as asynchronous systems, remove many problems associated with the clock signal of synchronous systems." *Id.*, col. 1, lines 49-51. Thus, Paver clearly describes techniques for controlling the speed of functional units without using a clock signal. *See Paver*, claim 10 (stating "wherein

power determination device modifies a cycle time *without a clock signal*") and claim 19 (stating "wherein an execution speed of the asynchronous system is based on the power consumption level *without using a clock signal*")(emphasis added). Thus, rather than referring to a clock cycle, the "cycle time" of Paver instead refers to the operational period (or the inverse frequency of operation) of a functional unit used to perform a certain step. *See, e.g., Paver*, col. 5, lines 33-56; *see also Paver*, claims 6, 7, 9, 11, 15 and 20. Paver further teaches that the "cycle time" may be adjusted by adding a delay into a handshake loop that controls an operational period of a functional unit. *See Id.*, col. 6, lines 15-22.

Accordingly, because the disclosure of Paver is clearly directed to an asynchronous system that does not use a clock signal to control the performance of the system and because Paver fails to disclose or suggest modifying a clock signal based on an operating characteristic of the system, Paver necessarily fails to disclose or suggest the features of adjusting a system characteristic based on an operating characteristic, wherein a power consumption of a system is modified based on the system characteristic and *wherein adjusting the system characteristic includes modifying a clock speed.* The Office Action does not assert that Bucher or Gupta disclose or suggest these features. The Office Action therefore fails to establish that the cited references, alone or in combination, disclose or suggest each and every feature of claim 11, as well as each and every feature of claims 12 and 13 at least by virtue of their dependency from claim 11. Moreover, these dependent claims recite additional features neither disclosed nor suggested by the cited references.

In view of the foregoing, it is respectfully submitted that the rejections of claims 11-13 are improper at this time and the withdrawal of these rejections therefore is respectfully requested.

Rejections of Claims 38 and 41-43

At page 3 of the Office Action, claims 38, 42 and 43 were rejected under 35 U.S.C. Section 102(b) as being anticipated by Paver. At page 5 of the Office Action, claim 41 was rejected under 35 U.S.C. Section 103(a) as being unpatentable over Paver in view of Bucher. These rejections are respectfully traversed.

Claim 38, from which claims 41-43 depend, has been amended to remove reference to the features of the operating characteristic comprising a buffer fullness or a type of instructions. Accordingly, claim 38 presently recites the features of a program of instructions to manipulate a processor to identify a rate of change in a number of pending instructions stored in an instruction buffer, and adjust a system characteristic based on the rate of change in the number of pending instructions, wherein a power consumption of a system is modified based on the system characteristic. The Office Action rejected claim 38 on the same rationale as described above with respect to claim 1. However, as also described above with respect to claim 1, Paver does not disclose or suggest the identification of a rate of change in a number of pending instructions stored in an instruction buffer, nor does Paver disclose or suggest adjusting a system characteristic based on the rate of change in the number of pending instructions. Moreover, the Office Action does not establish that Paver discloses a program of instructions that manipulate a data processor to identify a rate in change in the number of pending instructions and to adjust a system characteristic based on the rate in change in the number of pending instructions as recited by claim 38. The Office Action does not assert that Bucher discloses or suggests these features. Accordingly, it is respectfully submitted that the Office Action fails to establish that the cited references disclose or suggest, alone or in combination, each and every feature of claim 38, as well as each and every feature of claims 41-43 at least by virtue of their dependency from claim 38. Moreover, these dependent claims recite additional features neither disclosed nor suggested by the cited references. To illustrate, claim 42 recites the additional features of wherein the system characteristic includes a clock speed used to process the instructions. As noted above with respect to claim 11, none of the cited references disclose or suggest that the adjusted system characteristic includes a clock speed as provided by claim 42.

In view of the foregoing, it is respectfully submitted that the rejections of claims 38, 41 and 43 are improper at this time and the withdrawal of these rejections therefore is respectfully requested.

Conclusion

It is respectfully submitted that the present application is in condition for allowance and an early indication of the same is courteously solicited. The Examiner is respectfully requested

to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

The Commissioner is hereby authorized to charge any fees that may be required, or credit any overpayment, to Deposit Account Number 50-0441.

Respectfully submitted,

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Date

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